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REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested.

By the above-made amendments, independent claim 1 was amended to further highlight the circuit construction of an individual memory cell of the set forth "plurality of memory cells for storing digital display data." The latter are separate from the set forth "plurality of display pixels [which are] arranged in a matrix to provide image display" according to the image display apparatus of the present invention. It is submitted, the invention as currently set forth in independent claim 1, as well as with regard to the corresponding dependent claims thereof, as well as that set forth in independent claim 28, could not have been rendered obvious as alleged in the outstanding rejections. Therefore, insofar as presently applicable, the newly formulated art rejections, including the rejection of claims 1, 9, 17, 23 and 26 under 35 U.S.C. §103(a), allegedly, over the combination of Moriyama (USP 5,583,533) in view of Yamaguchi et al (USP 5,627,557), the rejection of claims 2-4, 20, 24 and 27 under 35 U.S.C. §103(a), allegedly, over the same combination of Moriyama and Yamaguchi et al and further in view of Parks (USP 5,471,225), the rejection of claims 10, 19 and 28 under 35 U.S.C. §103(a), allegedly, over the combination of Moriyama in view of Zhang et al (USP 6,611,861), and additionally, the rejection of claims 10 and 19 under 35 U.S.C. §103(a), allegedly, over the above-made combination of Moriyama and Yamaguchi et al in view of Zhang et al (*supra*), are traversed and withdrawal of the same is respectfully requested.

The present invention is directed to an image display apparatus facilitating the display of an image while realizing, among the attributes thereof, low power consumption. This is realized even when capacitance is used in the memory cells for storing an image data. Regarding independent claim 1, the invention as currently set forth, is an image display apparatus comprising:

> a plurality of signal lines;
>
> a plurality of display pixels arranged in a matrix to provide image display, each of said display pixels comprising a pixel electrode connected to said each of the plurality of signal lines via a pixel switch;
>
> a plurality of data lines;
>
> a plurality of memory cells for storing digital display data;
>
> an image signal generating circuit for outputting an image signal to the signal lines based on said digital display data inputted from the plurality of memory cells via the data lines; and
>
> wherein each of the plurality of memory cells comprises a memory switch connected to one of said data lines; a memory capacitor connected to said memory switch; and a field-effect transistor of which a source-drain path thereof is provided between a first node and a second node coupled to a corresponding one of said data lines,
>
> wherein one electrode of said memory capacitor is connected to a gate of said field-effect transistor and another electrode of said memory capacitor is connected to said second node, and
>
> wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node.

Examples of the invention according to claim 1 are discussed in the specification such as it relates to Figs. 1+, etc. of the present application, although not to be construed as being limited thereto. In the example embodiment of Fig. 1, reference 5 relates to the set forth plurality of **signal lines** connected to the **display pixels** 10 which are arranged in the matrix, in which each display pixel 10

comprises **pixel electrode** (see also for example Fig. 6 regarding layout of the pixel, as one example) connected to a respective signal line 5 via a **pixel switch** 2. In Fig. 1, further, reference 22 relates to the set forth **plurality of data lines** and the memory cells 11, which are arranged in a matrix such as in connection with the frame memory which stores display data, represent an example of the set forth **plurality of memory cells for storing digital display data**. In Fig. 1 of the drawings, although not to be construed as being limited thereto, each memory cell 11 is for a three-bit image data.

According to base claim 1, a key aspect thereof concerns the circuit construction of the individual memory cells of the set forth plurality of memory cells. In this regard, the invention calls for the following:

> wherein each of the plurality of memory cells comprises a memory switch connected to one of said data lines; a memory capacitor connected to said memory switch; and a field-effect transistor of which a source-drain path thereof is provided between a first node and a second node coupled to a corresponding one of said data lines,
>
> wherein one electrode of said memory capacitor is connected to a gate of said field-effect transistor and another electrode of said memory capacitor is connected to said second node, and
>
> wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node.

Examples of a circuit construction of such memory cells are shown in Fig. 1 and discussed with regard to Figs. 2 and 7 of the drawings such as they relate to each bit of a multi-bit memory cell 11 (in Fig.) in which the set forth **memory switch** which is connected to one of the data lines 22 is shown by FET switch 33, the **memory capacitor** which is connected to the memory switch is shown by numeral 31, and FET amplifier 32 relates to the set forth **field-effect transistor**

having its source-drain path provided between a first node and a second node coupled to a corresponding data line (this can be seen by the coupling of the source side of FET 32 to the data line 22 via the diode connected FET 34). Figs. 10 and 15 are other disclosed examples of memory cells for storing digital display data according to the present invention, although not to be construed as being limited thereto. Consistent with the last 'wherein' clause in claim 1, in Fig.1, a predetermined voltage is supplied through FET 61, provided on the drain side of FET 32, i.e., the first node side. Regarding the example memory cell construction featured in Fig. 2 or 10 and operation thereof, see the related discussion beginning on page 13, paragraph [0045] of the Third Substitute Specification.

It is alleged in the outstanding rejection of independent claim 1 that Moriyama discloses all of the limitations thereof except with regard to the details of the circuit construction of the individual memory cells with regard to the set forth *plurality of memory cells for storing digital display data*. In this regard, the Examiner has alleged, in view of Yamaguchi et al, that it would "[i]t would have obvious...to include the configuration of the memory cells as taught by Yamaguchi into Moriyama et al...(Yamaguchi, col. 5, lines 16-28)." It is submitted, however, a memory cell construction (for storing digital display data) according to claim 1 not only was not disclosed nor suggested by Moriyama, but, also could not have been achievable even over the combined teachings of Moriyama and Yamaguchi et al. For example, as is stated in column 6, line 39, etc., of Moriyama, "Fig. 8 illustrates an equivalent circuit of each matrix cell of the active matrix liquid crystal display illustrated in Fig. 7." Moriyama further states that "[t]he liquid crystal cell capacitor 15 comprises the pixel electrode 13 and an opposite electrode COM"

(col. 6, lines 50-52). On the other hand, the invention according to claim 1 distinguishes the set forth *plurality of memory cells for storing digital display data* from the set forth *plurality of display pixels arranged in a matrix to provide image display*. From the context of independent claim 1, an image pixel which is represented by a display pixel (e.g., 10 in Fig. 1, etc.) is separate from that of a memory cell (e.g., 11), the constituent elements of which and specific connections thereof are now further defined. Such it is submitted was neither taught nor could have been realized even over the combined teachings of Moriyama and Yamaguchi et al.

Assuming, *arguendo*, that Yamaguchi et al discloses a memory cell circuit construction that is usable in Moriyama, the circuit construction is still different from that of present claim 1. For example, according to claim 1, *each memory cell comprises a memory switch connected to one of the data lines, a memory capacitor connected to the memory switch and a field effect transistor having its source-drain path thereof provided between the first node and a second node coupled to a corresponding one of the data lines, in which one electrode of the memory cell is connected to a gate of the field effect transistor and another electrode of the memory capacitor is connected to the second node*. As discussed above, examples of this are illustrated with regard to at least Figs. 1, 2, and 10 of the drawings, although not to be construed as being limited thereto.

In the paragraph bridging pages 3 and 4 of the Detailed Action, it is alleged that Yamaguchi et al teach Applicants' claimed limitation that the source - drain path of the set forth field effect transistor *is provided between a first node and a second node coupled to a corresponding one of said data lines* (Fig. 2). Based on

the discussion in the paragraph bridging pages 3 and 4 of the detailed action, however, it is not clear what is considered as "a second node", as is called for by the present invention. It is clearly apparent that none of the voltage lines associated with V_{EE}, V_{COM} and GND can be considered as corresponding to the data line. Further, assuming the convention employed in the rejection and that the memory capacitor is shown by CH in Fig. 2 of Yamaguchi et al, the referred to *a second node* could only be satisfied by V_{COM}. However, in Yamaguchi et al, V_{COM} is defined as having a value, e.g., an intermediate value, between V_{EE}, which is applied to the common line 3, and GND. According to claim 1, also, the data line is the structural element for transmitting the data to the memory cell (e.g., 22 in Figs. 1, 2 and 10). On the other hand, in accordance with Yamaguchi et al's disclosure, the data line can only correspond to what is referred as the "Data Signal" (see Fig. 2). As is now set forth in independent claim 1, *each of the plurality of memory cells comprises a memory switch connected to one of said data lines* and, moreover, *the source-drain path of the set forth field-effect transistor is provided between a first node and a second node coupled to a corresponding one of said data line*, in clear contradistinction with that taught by Yamaguchi et al.

It is submitted, in view of the deficiencies in Moriyama and noting also the above-noted structural differences between Yamaguchi et al's schemed circuit and the present invention, and even when Moriyama and Yamaguchi et al are considered in combination, the invention according to claim 1, could not have been rendered obvious as alleged in the outstanding rejection to claim 1. For the same and similar reasons, also, the invention according to claims 9, 17, 23 and

26, Applicants submit, is patentable over the combined teachings of Moriyama and Yamaguchi et al.

It is submitted, claims 2-4, 20, 24 and 27, which further limit the invention according to claim 1, are, likewise, patentable for the same and similar reasons as that discussed above. In this regard, it is noted that Parks was cited concerning the pixel construction and other structural particulars of an LCD. In other words, the combination of Moriyama in view of Yamaguchi et al as further combined with Parks still failed to overcome the above-noted deficiencies.

As to claims 10 and 19, which further limit the circuit construction of the individual memory cells of the image display apparatus according to claim 1, the combined teachings of Moriyama in view of Zhang et al, it is submitted, could not have led to the present invention noting that both Moriyama and Zhang et al, even when considered in combination, failed to teach a memory cell circuit construction as that set forth in base claim 1 and as further characterized in intervening claim 17. Therefore, for at least the above given reasons, the invention according to claims 10 and 19 also could not have been rendered obvious in the manner alleged in the outstanding rejection. Likewise, also, even when considering the combined teachings of Moriyama and Yamaguchi et al, as further combined with Zhang et al, the invention according to claims 10 and 19 still could not have been rendered obvious, for the same and similar reasons as that discussed above.

It is submitted, the invention according to claim 28 is also defining over the combined teachings of Moriyama in view of Zhang et al. The following discussion is supportive of this.

It is admitted in the rejection that, among the set forth aspects according to claim 28, Moriyama fails to teach using a boron-doped polycrystalline Si (poly-si) thin-film resistor as a gray scale voltage generating resistor associated with the reference voltage generator circuit of the D-to-A converter (see the fourth paragraph on page 8 of the Detailed Action). It is alleged in the rejection, however, that Zhang et al discloses voltage generation using polycrystalline Si in the manner set forth in claim 28. According to the present invention, the polycrystalline Si thin-film is not prepared using the phosphorus doped structure and the arsenic doped structure. Rather, according to claim 28, the invention calls for a reference voltage generating circuit (of the D-to-A converter) using *a boron-doped polycrystalline Si thin-film resistor as a gray scale voltage generating resistor*. Such, it is submitted, was not taught by Zhang et al or, for that matter, even over the combined teachings of Moriyama and Zhang et al.

When applying the combined teachings of Yamaguchi and Zhang et al, the resistance that would be realized would likely be prepared using phosphorus and arsenic-doped poly-si thin film. On the other hand, the poly-si thin-film resistor, according to claim 28, is necessarily a boron-doped poly-si thin-film resistor which leads to unexpected favorable results as compared with, for example, the phosphorus-doped poly-si material. Related discussion regarding such thin film resistor construction is given in paragraphs [0038] – [0040] on pages 9-11 of the Third Substitute Specification. In particular, note the favorable attributes associated with the boron-doped poly-si thin-film resistor [having low-dispersion rate resistance], discussed in paragraph [0040] and Table 2 in the specification. It is submitted, such could not have been realizable in view of Zhang et al or, for that

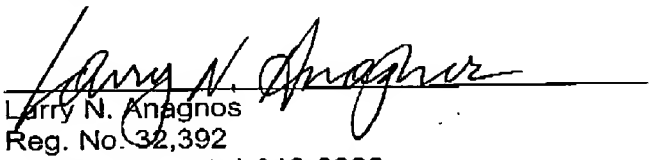
matter, even over the combined teachings of Moriyama and Zhang et al. That is, for at least the above reasons, the invention according to claim 28, it is submitted, could not have been achieved from the combined teachings of Moriyama and Zhang et al.

Therefore, in view of the above-made amendments, together with these accompanying remarks, withdrawal of the outstanding rejections as well as favorable action on the pending claims, i.e., claims 1-4, 9, 10, 17, 19, 20, 23, 24 and 26-28, together with an early formal notification of allowance of the above-identified application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. § 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (503.40029X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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Enclosures

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